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EXAMINER
VOCKRODT, JEFF B

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/964,127	Applicant(s) ASSADERAGHI ET AL.	
	Examiner Jeff Vockrodt	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 3-6-02 .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This office action is in response to the information disclosure statement filed on March 6, 2002. Claims 1-20 are pending.

Claim Objections

Claims 12-20 are objected to because of the following informalities:

Steps (a) and (d) of claim 12 are incompatible with the corresponding disclosure in the specification (reference by paragraph number will be made to the pre grant pub US 2002/0008290). Claim 12, step (a), requires concurrently forming a capacitor device body and a plurality of additional device bodies using a first conductivity type dopant (say for instance n-type). This corresponds to the specification at ¶ 0037, which states that the n-well material for the capacitor also forms p-type transistor (i.e., PMOS) bodies (well regions) elsewhere on the chip. However, step (d) requires the source and drain regions of the additional device bodies to be formed using the first conductivity type dopant (n-type) concurrently with the lateral regions of the capacitor device. Transistors having n-type source/drain regions are NMOS devices and not PMOS devices. Insofar as the claim requires transistors with a first dopant type well and a first dopant type source/drain, the claim is inconsistent with what has been disclosed in the specification. Accordingly, claims 12-17 are objected to under 37 C.F.R. § 1.75(d)(1). For examination purposes, with respect to comparison with prior art below, I will assume that the claim does not require the first lateral region, second lateral region, each respective drain region, and each respective source region being formed using the same type of dopant material. Claim 18 similarly requires the first and second lateral regions to be analogous to the source/drain regions of a transistor having a well region of the same conductivity as the capacitor body. Claims 19-20 incorporate this defect by way of reference to claim 18. Accordingly, claims 18-20 are objected to under 37 C.F.R. § 1.75(d)(1).

Appropriate correction is required.

Claim R j ctions - 35 USC § 112

The following are quotations from the first and second paragraphs of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
>
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 12 seems to require a transistor that is formed having the same conductivity source and drain region as the well region within which it is formed. An essential defining characteristic of a source/drain region however is that it is opposite the conductivity of the body in which it is formed. This internal inconsistency renders the scope of the claim vague and indefinite. Claims 13-17 incorporate this defect by way of reference to claim 12. Claim 18 similarly requires the first and second lateral regions to be analogous to the source/drain regions of a transistor having a well region of the same conductivity as the capacitor body. Claims 19-20 incorporate this defect by way of reference to claim 18.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 18-19 are rejected under 35 U.S.C. 102(b) insofar as understood as being anticipated by U.S. Pat. No. 5,576,565 ("Yamaguchi").

Claim 18 reads on Yamaguchi as follows: A method for improving the frequency response of a decoupling capacitor (100; Fig. 4a) in an integrated circuit, the decoupling capacitor including a device body (n-well 4 Rec) analogous to the device body (n-well 4 Rem)of a transistor included in the integrated circuit and being formed using a first type impurity material, the decoupling capacitor further including first and second lateral regions (12b) analogous[1] to the source and drain regions of the transistor (74) included in the integrated circuit chip, the method comprising the step of: (a) adding additional first type impurity material (As implant shown in Fig. 4b that is selective to the capacitor) to an area in the substrate for the decoupling capacitor device body, the additional first type impurity material resulting in a region on the substrate for the decoupling capacitor device body that is more highly doped than a region on the substrate for the transistor device body.

Claim 19. The method of claim 18 wherein the decoupling capacitor device body is formed in an N-well (4) formed on a P-type substrate (1). (Fig. 4a)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

[1] It is assumed here that the claim is intended to cover, inter alia, a device wherein source and drain regions of the transistor that have analogous n-wells with the capacitor are p-type and thus have the opposite type impurity as the body of the capacitor. See treatment of claims 12-20 above with regard to 35 U.S.C. § 112 and 37 C.F.R. § 1.75(d)(1).

Claims 1, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,266,821 ("Chern '821") in view of U.S. Pat. No. 4,929,989 ("Hayano").

Chern '821 teaches a depletion type MOS capacitor that is used as a decoupling capacitor.

Claim 1 corresponds to Chern '821 as follows (differences underlined): A method of forming a capacitor (Fig. 9) on a semiconductor substrate, the method including the steps of: (a) forming a device body (N-WELL; Fig. 9) in the semiconductor substrate using a first type (N-type) of dopant material; (b) forming a dielectric layer ("oxide"; col. 3, ll. 10-11) over the device body; (c) forming an electrode layer (poly 25; compare Figs. 4 and 9) over the dielectric layer in an area defined by an upper surface of the device body (Fig. 9); (d) forming a first lateral region (leftmost N+ diffusion; Fig. 9)in the semiconductor substrate along a first lateral side of the device body (N-WELL), the first lateral region being in electrical contact with the device body along the first lateral side of the device body and containing the first type of dopant material at a level relatively higher than is characteristic of the device body (Fig. 9); (e) forming a second lateral region (rightmost N+ diffusion; Fig. 9) in the semiconductor substrate along a second lateral side of the device body opposite the first lateral side, the second lateral region being in electrical contact with the device body along the second lateral side of the device body and containing the first type of dopant material at a level relatively higher than is characteristic of the device body (N+ versus N); (f) forming an insulating layer over the electrode layer, first lateral region, and second lateral region; (g) electrically connecting the first and second lateral regions (15; Fig. 4) to a first supply voltage potential at a first longitudinal end of the device body (connection to Vss; Figs. 4 and 8); and (h) electrically connecting the electrode layer (25; Fig. 4) to a second supply voltage potential at a second longitudinal end of the device body opposite to the first longitudinal end of the device body (connection to Vcc; Figs. 4 and 8).

Chern '821 discloses that the busses to which the first and second lateral regions and the electrode are connected, "are typically metallization layers," col. 3, ll. 15, but does not state the claim requirement of "(f) forming an insulating layer over the electrode layer, first lateral region, and second lateral region." It is noted, however, that the black squares in Fig. 4 suggests connecting the metallization to the device at those locations. The claim limitations would be fully met by depositing an insulating material over the entire substrate surface prior to forming the metallization layers for the busses in the process of Chern '821.

Hayano teaches MOS type decoupling capacitors connected between Vcc and ground and interconnected using a metallization structure (Figs. 1A-1B). Hayano teaches interposing an insulating layer (5) between the metallization (37, 39) and upper (34) and lower (3) electrodes. One of ordinary skill in the art would recognize from Hayano that using an insulating layer allows for more sophisticated interconnect layout and enables contacting the device through contact holes at predetermined locations.

Chern '821 and Hayano are analogous art and in applicant's field of endeavor -- MOS type decoupling capacitors.

It would have been obvious to one of ordinary skill in the art at the time of the invention to deposit an insulating layer over the entire decoupling capacitor before forming the metallization layer in the process of Chern '821. One of ordinary skill in the art would have been motivated to interpose an insulating layer between the metallization and the MOS capacitor to provide for more sophisticated interconnect layout and enable contacting the device through contact holes at predetermined locations as taught by Hayano.

Claim 4. The method of claim 1 further including the step of forming a first end region (region where contacts to Vss are made; Fig. 8) in the semiconductor substrate abutting the first longitudinal end of the device body and contacting the first and second lateral regions adjacent

to the first longitudinal end of the device body, the first end region being formed using the first type of dopant material.

Claim 5. The method of claim 4 wherein the step of electrically connecting the first lateral region and the second lateral region to the first supply voltage potential comprises forming ground potential contacts to the first end region (This is shown by symbols on Fig. 9 and the actual contact region in Fig. 8).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chern '821 and Hayano as applied to claims 1, 4, and 5 above, and further in view of U.S. Pat. No. 6,018,175 ("Kao") (cited in IDS filed March 6, 2002).

Claim 2. The method of claim 1 wherein the first type of dopant material comprises N-type material and the step of forming the device body includes implanting the N-type material in a bulk P-type semiconductor substrate. (Chern '821; Fig. 9).

The only difference between Chern '821 and Hayano as applied to claims 1, 4, and 5 above and the subject matter of claim 2 is that Chern '821 does not teach whether the dopant regions, specifically the N-WELL region, is formed using ion implantation.

Kao teaches a well-implant step after forming the oxide and before forming the first mask (col. 5, ll. 18-28) in forming a depletion mode capacitor.

It would have been obvious to one of ordinary skill in the art at the time of the invention to carry out the formation of the N-WELL region using ion implantation in the process of Chern '821 and Hayano. One of ordinary skill in the art would have been motivated to use ion implantation by Kao's teaching that well-implantation was well known and desirable for forming n-well regions in MOS decoupling capacitors.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentabl ov r Chern '821 and Hayano as appli d to claims 1, 4, and 5 abov , and furth r in vi w of U.S. Pat. No. 5,965,928 ("Nagura").

Chern '821 differs from claim 3 by not teaching "(b) wherein the step of forming the device body includes performing an additional N-type material implantation in a selected area of the well." Instead, Chern '821 teaches only one doping step for forming the body of the capacitor.

Nagura teaches an improvement on MOS capacitors (Fig. 1E) that includes forming n-type diffusion regions (17; Fig. 1F) in n-type well regions (4) between lateral doping regions (20). Nagura teaches that this suppresses the voltage dependence of the capacitance (e.g., col. 3, ll. 59-61).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide a step for forming diffusion region in the device by implanting an additional n-type material into the well in the process taught by Chern '821 and Hayano. One of ordinary skill in the art would have been motivated to include this step because such structure was known to reduce the voltage dependence of the capacitance as taught by Nagura.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chern '821 and Hayano as applied to claims 1, 4, and 5 above, and further in view of U.S. Pat. No. 6,034,388 ("Brown").

Claim 6. The method of claim 1 further including the steps of forming a buried oxide layer in the semiconductor substrate and forming side oxide regions in the semiconductor substrate in areas bounding an area for the capacitor, the steps of forming the buried oxide layer and side oxide regions being performed prior to forming the device body. Claim 6 differs

from Chern '821 and Hayano as applied above by requiring a buried oxide layer and side oxide regions.

Brown teaches forming a depletion mode capacitor in a SOI substrate that includes buried oxide regions (522; Fig. 13) and side oxide regions (shallow trench isolation 170; Fig. 13) which are formed prior to forming the device body (520). Brown teaches that using SOI increases the resistance (col. 14, ll. 38-39).

Chern '821, Hayano, and Brown are within the same field of endeavor as applicant -- MOS type decoupling capacitors.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the decoupling capacitor of Chern '821 and Hayano on a SOI substrate having side oxide regions formed prior to the body formation. One of ordinary skill in the art would have been motivated to use SOI by the expectation of increased resistance as taught by Brown.

Claims 7-8 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chern '821, Hayano, and Brown as applied to claim 6 above, and further in view of Kao.

Chern '821, Hayano, and Brown differ from claims 7-8 and 10-11 in that Chern '821 does not teach ion implantation and is silent as to the doping method. Kao as applied to claim 2 above teaches how to use ion implantation to form the device of Chern '821. The findings with respect to claim 2 above are incorporated in this section. It would have been obvious to one of ordinary skill in the art at the time of the invention to carry out the formation of the N-WELL region using ion implantation in the process of Chern '821, Hayano, and Brown. One of ordinary skill in the art would have been motivated to use ion implantation by Kao's teaching that well-implantation was well known and desirable for forming n-well regions in MOS decoupling capacitors.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chern '821, Hayano, Brown, and Kao as applied to claims 7-8 and 10-11 above, and further in view of U.S. Pat. No. 5,965,928 ("Nagura").

Chern '821 differs from claim 9 by not teaching "(b) wherein the step of forming the device body includes performing an additional N-type material implantation in a selected area of the well." Instead, Chern '821 teaches only one doping step for forming the body of the capacitor.

Nagura teaches an improvement on MOS capacitors (Fig. 1E) that includes forming n-type diffusion regions (17; Fig. 1F) in n-type well regions (4) between lateral doping regions (20). Nagura teaches that this suppresses the voltage dependence of the capacitance (e.g., col. 3, ll. 59-61).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide a step for forming diffusion region in the device by implanting an additional n-type material into the well in the process taught by Chern '821 and Hayano. One of ordinary skill in the art would have been motivated to include this step because such structure was known to reduce the voltage dependence of the capacitance as taught by Nagura.

Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chern '821 and Hayano as applied to claims 1, 4, and 5 above, and further in view of U.S. Pat. No. 5,032,892 ("Chern '892).

Claim 12 differs from Chern '821 since Chern '821 does not teach concurrently forming a capacitor device body and a plurality of additional device bodies and does not teach step (d) of claim 12.

Chern '892 teaches forming a PMOS transistor (121, 131, 132) while forming a n-doped depletion mode capacitor (139). Chern '892 corresponds to step (d) of claim 12 as follows: (d)

forming a first lateral region (134) and a second lateral region (135) in the semiconductor substrate along opposite lateral sides of the capacitor device body (113) and concurrently forming a respective drain region (131) and a respective source region (132) in the semiconductor substrate along opposite sides of each respective additional device body (111), the first lateral region (134), second lateral region (135), each respective drain region (131), and each respective source region (132) being formed using the first type of dopant material[2] at a level relatively higher (indicated by "+" signs, e.g. n+) than is characteristic of the capacitor device body (113) and each respective additional device body (111). Chern '892 teaches that "a separate depletion mask is not needed in a CMOS process because one can introduce n-type doping to form the n doped barrier during the n well implant step" (¶ bridging cols. 4-5).

It would have been obvious to one of ordinary skill in the art at the time of the invention to concurrently form a capacitor device body (n doped barrier) and a plurality of additional device bodies (n wells) in the process of Chern '821 and Hayano. One of ordinary skill in the art would have been motivated to make this modification to eliminate the separate depletion masking step as taught by Chern '892.

Claim 14. The method of claim 12 wherein the step of forming the first lateral region, second lateral region, each drain region, and each source region also includes concurrently forming a first end region (region where contacts to Vss are made; Chern '821, Fig. 8) in the semiconductor substrate abutting the first longitudinal end of the capacitor device body and contacting the first and second lateral regions adjacent to the first longitudinal end of the capacitor device body.

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[2] It is assumed here that the claim is intended to cover, inter alia, a device wherein source and drain regions of the transistor that have analogous n-wells with the capacitor are p-type and thus have the opposite type impurity as the body of the capacitor. See treatment of claims 12-20 above with regard to 35 U.S.C. § 112 and 37 C.F.R. § 1.75(d)(1).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chern '821, Hayano, and Chern '892 as applied to claims 12 and 14 above, and further in view of Kao.

Claim 13 requires implanting the dopants. See treatment of claim 2 in view of Kao above for reasons underlying this ground of rejection.

Conclusion

Any inquiry concerning communications from the examiner should be directed to Jeff Vockrodt at (703) 306-9144 who can be reached on weekdays from 9:30 am to 5:00 pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (703) 308-4905.

The fax numbers for this Group are (703) 305-3432, (703) 308-7722, (703) 305-3431, and (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist at (703) 308-0956.

March 24, 2003

J. Vockrodt

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